Affirmation of Election

The applicant wishes to affirm the election of species I claims 1-5, 8, 9 and 12-14. Accordingly, claims 6, 7, 10 and 11 are canceled.

Drawing Objections

The Examiner objected to figures 2a and 2b, due to a number of inconsistencies which existed between the specification and the figures, and for other problems as well. In response, both the specification and the figures have been amended. Corrected versions of FIGs. 2a and 2b are enclosed, with the corrections indicated in red - new drawings with the indicated corrections incorporated will be submitted upon receipt of a Notice of Allowance. The specification has also been amended (as shown above) to make the text consistent with the corrected drawings. It is believed that these amendments address and resolve each of the Examiner's objections with respect to the drawings.

Claim Rejections under §103

Claims 1, 5, 8, 9 and 12-14 were rejected as obvious over a patent to Hou in view of a patent to Wilder et al.

In response, claims 1, 8 and 12 have been amended, as discussed below:

Claim 1

Claim 1 is directed to a photodetector array comprising a plurality of addressable pixels. Each pixel in the array must comprise:

- at least two photodiodes;

- a switching circuit which allows switching of at least one of the photodiodes between a first circuit and a second circuit, wherein the first circuit directly combines the outputs of said at least two photodiodes in parallel, and the second circuit

directly combines the output of the at least one photodiode in parallel with the output of a photodiode of a neighboring pixel in the array;

- such that the array is switchable between a high resolution and a low resolution pixel configuration, the pixel having an intrinsic capacitance which stores the combined photodiode outputs prior to their being read out, and

- an addressing circuit which enables the combined photodiode outputs stored on the pixel's intrinsic capacitance to be read out in response to an address input.

Thus, as amended, the photodetector array is arranged so that:

- the outputs of the at least two photodiodes making up a pixel can be combined in parallel, or
- the output of at least one of the pixel's two photodiodes can be combined with the photodiode of a neighboring pixel.

Each pixel in an array is "read out" to determine the amount of light which has impinged on the pixel. The amended claim 1 requires that the photodetector outputs be combined directly, prior to the pixel's being read out. This means that the photodetector outputs themselves must be connected together ("combined") before the pixel is read out.

The cited art is quite different. The patent to Hou discloses an array of passive pixels. Hou's passive pixels operate by first closing switches 304 to dump the outputs of photodetectors 302 to respective storage capacitors 306; switches 304 then open. When a photodetector output is to be read out, one of switches 308 is closed to connect the appropriate storage capacitor to amplifier 314.

Thus, Hou fails to disclose several essential elements of the amended claim 1. Claim 1 requires that the photodiode out-

puts be directly combined. It also required that the combined outputs be stored prior to their being read out. This results in the resolution of the pixel being established prior to its being read out.

Hou meets none of these requirements. His system does not combine the photodiode outputs directly - rather, it is his storage capacitor voltages that are combined. Furthermore, his capacitor voltages are not combined prior to their being read out - they are combined only after they are read out. This is true for the resolution as well - Hou's pixel resolution is established only after the capacitor voltages are read out.

These distinctions are significant. Hou's approach is only applicable to passive pixel systems, while the applicant's system is useful for either active pixel systems (as described in the specification) or passive systems. For a passive pixel system such as Hou's, only one row of stored pixel values are available at any given time; i.e., the values for the previous and subsequent rows are not available at the same time. Therefore, as Hou's system combines voltages from storage capacitors which are necessarily in a common row, Hou's approach is limited to use with one-dimensional arrays. In contrast, the applicant's system allows the combining of photodiode outputs from neighboring pixels - even if those pixels are in different rows - i.e., the photodetector array recited in the amended claim 1 can be used with two-dimensional arrays.

Note that the cited patent to Wilder does nothing to cure the deficiencies in the Hou patent. Wilder discusses pixel addressing, but says nothing about combining photodiode outputs to achieve various pixel resolution configurations.

As Hou and Wilder lack the above-noted essential elements of claim 1, it is improper to find that the amended claim 1 is obvious in view of them. The amended claim 1 is therefore allowable over Hou and Wilder.

The amended claim 1 is the parent of claim 5, which is therefore allowable along with claim 1.

Claim 8

Claim 8 is an independent claim which is directed to a photodetector array with selectable resolution. Claim 8 has been amended in the same fashion as was claim 1. As amended, the array of claim 8 comprises:

- a plurality of photodetectors;
- a switching circuit which configures neighboring photodetectors into pixels by directly summing at each pixel the outputs of multiple photodetectors into an aggregated pixel output, which is stored on the pixel's intrinsic capacitance prior to being read out;
- wherein the switching circuit is electronically switchable to aggregate the photodetector signals according to at least two different selectable pixellization schemes with differing resolutions; and
- a plurality of addressable interface circuits, each of which enables the aggregated pixel output stored on a respective pixel to be read out in response to an address input.

As with the amended claim 1, the patent to Hou fails to disclose several essential elements of the amended claim 8. Claim 8 requires that the photodetector outputs be directly summed. It also requires that the summed outputs be stored prior to their being read out. This results in the resolution of the pixel being established prior to its being read out.

Hou meets none of these requirements. His system does not combine the photodetector outputs directly - rather, it is his storage capacitor voltages that are combined. Furthermore, his capacitor voltages are not combined prior to their being read out - they are combined only after they are read out. This is true

for the resolution as well - Hou's pixel resolution is established only after the capacitor voltages are read out.

Furthermore, as noted above, Hou's approach is only applicable to passive pixel systems, while the applicant's claimed system is useful for either active pixel systems (as described in the specification) or passive systems. As a consequence, Hou's approach is limited to use with one-dimensional arrays. In contrast, the applicant's system allows the summing of photodetector outputs from neighboring pixels - even if those pixels are in different rows - i.e., the photodetector array recited in the amended claim 8 can be used with two-dimensional arrays.

As before, the cited patent to Wilder does nothing to cure the deficiencies in the Hou patent. Wilder discusses pixel addressing, but says nothing about combining photodiode outputs to achieve various pixel resolution configurations.

As Hou and Wilder lack the above-noted essential elements of claim 8, it is improper to find that the amended claim 8 is obvious in view of them. The amended claim 8 is therefore allowable over Hou and Wilder.

The amended claim 8 is the parent of claim 9, which is therefore allowable along with claim 8.

Claim 12

Claim 12 is an independent claim which is directed to a photodetector array. Claim 12 has been amended in the same fashion as were claims 1 and 8. As amended, claim 12 is directed to a photodetector array which comprises:

- a plurality of pixels, each of which comprises an association of at least two subpixels;
- wherein the outputs of said subpixels are switchably combined into at least two different grouping arrangements, to give at least two different selectable pixel configurations;

- each pixel having an intrinsic capacitance which stores the combined subpixel outputs prior to their being read out; and
- an addressing circuit which enables the combined subpixel outputs stored on the pixel's intrinsic capacitance to be read out in response to an address input.

As with amended claims 1 and 8, the patent to Hou fails to disclose several essential elements of the amended claim 12. Claim 12 requires that the subpixel outputs be combined - not the storage capacitor outputs. It also requires that the combined outputs be stored prior to their being read out. This results in the resolution of the pixel being established prior to its being read out.

Hou's system does not combine the photodetector outputs - rather, it is his storage capacitor voltages that are combined. Furthermore, his capacitor voltages are combined only after they are read out. This is true for the resolution as well - Hou's pixel resolution is established only after the capacitor voltages are read out. Hou's approach is only applicable to passive pixel systems, while the applicant's claimed system is useful for either active or passive pixel systems. As a consequence, Hou's approach is limited to use with one-dimensional arrays. In contrast, the applicant's system allows the outputs of neighboring subpixels to be combined - even if those subpixels are in different rows - i.e., the photodetector array recited in the amended claim 12 can be used with two-dimensional arrays.

As before, the cited patent to Wilder does nothing to cure the deficiencies in the Hou patent. Wilder discusses pixel addressing, but says nothing about combining photodiode outputs to achieve various pixel resolution configurations.

As Hou and Wilder lack the above-noted essential elements of claim 12, it is improper to find that the amended claim 12 is obvious in view of them. The amended claim 12 is therefore al-

lowable over Hou and Wilder.

The amended claim 12 is the parent of claims 13 and 14, which are therefore allowable along with claim 12.

Claims 2-4 were rejected as obvious over Hou and Wilder in view of Orava.

The amended claim 1 is the parent of claims 2-3, which are therefore allowable along with claim 1. As the limitation of claim 4 has been incorporated into claim 1, claim 4 has been canceled.

A new claim (claim 15) has been added which specifies a two-dimensional array of pixels, and defines two different grouping arrangements: one which combines the outputs of two adjacent subpixels in a given vertical column, and the other of which combines the outputs of three adjacent subpixels in said given vertical column. Nothing analogous to this arrangement is disclosed in any of the cited art, and thus claim 15 is allowable over the Hou, Wilder and Orava.

All of the claims presently in the application are believed to be in proper form for allowance. A Notice of Allowance is respectfully requested.

Respectfully submitted,

April 22, 2002

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Attachment A:

Amended specification with insertions and deletions indicated:

Paragraphs between page 6, line 16 and page 7, line 29:

FIG. 2a schematically shows the circuits of two exemplary pixels 30 and 32, each in accordance with the invention. Each pixel includes two photodiodes: PD1 and PD2 pertain to pixel 30, while PD3 and PD4 pertain to pixel 32. (The photodiodes PD1 and PD2 correspond to 20a and 20b on the plan of FIG. 1.) A reset FET [Q_{rs}] Q_{rs1} has its source connected to the cathode of [PD 1] PD1 and gate connected to [RS1] a reset line RESET #1. Thus, a signal on [RS1] RESET #1 can be used to reset the circuit by discharging any charge accumulated from photodiode PD1. Buffer/interface FETs Q2 and Q3 are connected in a source follower/common gate two stage buffer amplifier circuit, which allows the photodiode voltage to be read when [the] a select signal [Sel1] SELECT #1 is set high. When the interface amplifier is off, charge from photodiodes PD1 and PD2 accumulates across the intrinsic capacitance (primarily that of the PDs themselves) until it is read by enabling [Sel1] SELECT #1. Similarly, pixel 32 includes a reset FET Q_{rs2} connected to PD3 which is controlled by a reset line RESET #2, and buffer/interface FETs Q4 and Q5 which allow the voltage on photodiode PD3 to be read when a select signal SELECT #2 is set high.

Switches [s1] S1 and [s2] S2 are preferably high impedance, electronic switches (suitably CMOS FET switches) which allow the photodiodes PD1 and PD2 to be connected in either of two configurations, as selected by control signals. [In the position shown,] For example, both photodiodes from pixel 30, PD1 and PD2, [are] can be connected in parallel, so that the pixel 30 accumulates signal from both photodiodes. The circuit in each (ad-

dressable) pixel is electronically switchable to the alternate switch position [(shown in phantom)]. [For example, pixel 32 is shown with] With the switches in the alternate position, [:] the photodiodes PD3 and PD4 [are] can be connected so that PD4 is connected in parallel with photodiodes PD1 and PD2 (part of neighboring pixel 30).

A particular circuit realization of FIG. 2a is shown in FIG. 2b. FETs [Q1] Q5 and [Q2] Q6 act as switches [s1] S1 and [s2] S2, respectively, to switch the photodiode signals as described in connection with FIG. 2a. The switching of pixel 30 is controlled by control signals VS1 and VS2 applied to the gates of [Q1] Q5 and [Q2] Q6. [;] Similarly, [while] the switching of pixel 32 is controlled by control signals VS3 and VS4, which control FET switches Q7 and Q8, respectively. Pixel 32 is identical to 30 in its interface and detection circuitry, and indeed all the pixels in an imaging matrix may suitably include substantially the same circuit, although in operation the switches [s1] S1 and [s2] S2 may be differently set for various pixels.

Amended claims with insertions and deletions indicated.

1. (amended) A photodetector array comprising a plurality of addressable pixels, each pixel comprising:

at least two photodiodes;

a switching circuit which allows switching of at least one of said photodiodes between a first circuit and a second circuit;

wherein said first circuit directly combines the outputs of said at least two photodiodes [connects said at least two diodes] in parallel, and said second circuit directly combines the output of [connects] said at least one of said photodiodes in parallel with the output of a photodiode of a neighboring pixel in the array, whereby said array is switchable between a high resolution and a low resolution pixel configuration, said pixel having an

intrinsic capacitance which stores said combined photodiode outputs prior to their being read out, and

an addressing circuit which enables the combined photodiode outputs stored on said pixel's intrinsic capacitance to be read out in response to an address input.

8. (amended) A photodetector array with selectable resolution, comprising:

[A]a plurality of photodetectors;

[a plurality of addressable interface circuits;]

a switching circuit which configures neighboring ones of said photodetectors into pixels by directly summing at each pixel [multiple photodetector signals] the outputs of multiple photodetectors into an aggregated pixel output, said aggregated pixel output stored on said pixel's intrinsic capacitance prior to being read out;

wherein said switching circuit is electronically switchable to aggregate said photodetector signals according to at least two different selectable pixellization schemes with differing resolutions, and

a plurality of addressable interface circuits, each of which enables the aggregated pixel output stored on a respective one of said pixel's to be read out in response to an address input.

12. (amended) A photodetector array, comprising a plurality of pixels;

wherein each pixel comprises an association of at least two subpixels;

and wherein the outputs of said subpixels are switchably [associated] combined into at least two different grouping arrangements, to give at least two different selectable pixel configurations.

each of said pixels having an intrinsic capacitance which stores said combined subpixel outputs prior to their being read out, and

an addressing circuit which enables the combined subpixel outputs stored on said pixel's intrinsic capacitance to be read out in response to an address input.

15. The photodetector array of claim 12, wherein said array of pixels comprises a plurality of pixels arranged into at least three horizontal rows and vertical columns,

wherein said at least two different grouping arrangements comprises two different grouping arrangements, one of which combines the outputs of two adjacent subpixels in a given vertical column, and the other of which combines the outputs of three adjacent subpixels in said given vertical column.